IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having a top layer;

forming a first mask layer over the covering layer;

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and first mask layer;

removing etch residue from the second mask layer and first mask layer; and

selectively removing the first mask layer by a process different than the same etching process, wherein the second mask layer remains.

2. (Original) The method of claim 1, wherein providing a covering layer includes providing a covering layer including tantalum.

3. (Original) The method of claim 1, wherein forming a first mask layer includes forming a first mask layer including titanium nitride.

4. (Original) The method of claim 3, wherein selectively removing the first mask layer includes selectively removing the first mask layer including an ammonium peroxide mixture wet removal.

5. (Original) The method of claim 4, wherein selectively removing the first mask layer further includes removing footings disposed adjacently to the first mask layer and second mask layer.

6. (Original) The method of claim 1, wherein selectively removing the first mask layer includes a plasma removal.

7. (Original) The method of claim 1, wherein selectively removing the first mask layer includes ion milling.

8. (Currently Amended) The method of claim 1, wherein etching the second mask layer and first mask layer includes etching the second mask layer and partially etching the first mask layer, wherein the covering layer is not incorporated in an etch residue.

9. (Original) The method of claim 1, wherein forming a second mask layer includes forming a second mask layer including dielectric anti-reflective coating.

10. (Currently Amended) The method of claim 1, wherein forming a second mask layer includes forming a second mask layer including ~~siline~~ silicon oxides.

11. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having a top layer, wherein the covering layer includes tantalum;

forming a first mask layer over the covering layer;

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and first mask layer;

removing etch residue from the second mask layer and first mask layer; and

selectively removing the first mask layer by a process different than the same etching process, wherein the second mask layer remains.

12. (Original) The method of claim 11, wherein forming a first mask layer includes forming a first mask layer including titanium nitride.

13. (Original) The method of claim 12, wherein selectively removing the first mask layer includes selectively wet removing the first mask layer including an ammonium peroxide mixture wet removal.

14. (Original) The method of claim 13, wherein selectively removing the first mask layer further includes removing footings disposed adjacently to the first mask layer and second mask layer.

15. (Original) The method of claim 11, wherein selectively removing the first mask layer includes a removal process including plasma removal or ion milling.

16. (Currently Amended) The method of claim 11, wherein etching the second mask layer and first mask layer includes etching the second mask layer and partially etching the first mask layer, wherein the covering layer is not incorporated in an etch residue.

17. (Currently Amended) The method of claim 11, wherein forming a second mask layer includes forming a second mask layer including dielectric anti-reflective coating or ~~siline~~ silicon oxides.

18. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having a top layer;

forming a first mask layer over the covering layer, wherein the first mask layer includes titanium nitride;

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and first mask layer;

removing etch residue from the second mask layer and first mask layer; and

selectively removing the first mask layer by a process different than the same etching process, wherein the second mask layer remains.

19. (Original) The method of claim 18, wherein selectively removing the first mask layer includes selectively wet removing the first mask layer including an ammonium peroxide mixture wet removal.

20. (Original) The method of claim 19, wherein selectively removing the first mask layer further includes removing footings disposed adjacently to the first mask layer and second mask layer.

21. (Currently Amended) The method of claim 18, wherein etching the second mask layer and first mask layer includes etching the second mask layer and partially etching the first mask layer, wherein the covering layer is not incorporated in an etch residue.

22. (Currently Amended) The method of claim 18, wherein forming a second mask layer includes forming a second mask layer including dielectric anti-reflective coating or ~~siline~~ silicon oxides.

23. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having a top layer;

forming a first mask layer over the covering layer,

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and partially etching the first mask layer, wherein the covering layer is not incorporated in an etch residue;

removing etch residue from the second mask layer and first mask layer; and

selectively removing the first mask layer by a process different than the same etching process, wherein the second mask layer remains.

24. (Original) The method of claim 23, wherein forming a first mask layer includes forming a first mask layer including titanium nitride.

25. (Original) The method of claim 24, wherein selectively removing the first mask layer includes selectively wet removing the first mask layer including an ammonium peroxide mixture wet removal.

26. (Original) The method of claim 25, wherein selectively removing the first mask layer further includes removing footings disposed adjacently to the first mask layer and second mask layer.

27. (Currently Amended) The method of claim 23, wherein selectively removing the first mask layer includes a process including plasma removal or ion milling.[[.]]

28. (Currently Amended) The method of claim 23, wherein forming a second mask layer includes forming a second mask layer including dielectric anti-reflective coating or ~~siline~~ silicon oxides.

29. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having a top layer;

forming a first mask layer over the covering layer, wherein the first mask layer includes titanium nitride;

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and partially etching the first mask layer, wherein the covering layer is not incorporated in an etch residue;

removing etch residue from the second mask layer and first mask layer; and

selectively removing the first mask layer by a process different than the same etching process, wherein the second mask layer remains.

30. (Original) The method of claim 29, wherein providing a covering layer includes providing a covering layer including tantalum.

31. (Original) The method of claim 29, wherein selectively removing the first mask layer includes selectively wet removing the first mask layer including an ammonium peroxide mixture wet removal.

32. (Original) The method of claim 31, wherein selectively removing the first mask layer further includes removing footings disposed adjacently to the first mask layer and second mask layer.

33. (Original) The method of claim 29, wherein selectively removing the first mask layer includes a process including plasma removal or ion milling.

34. (Currently Amended) The method of claim 29, wherein forming a second mask layer includes forming a second mask layer including dielectric anti-reflective coating or ~~siline~~ silicon oxides.

35. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having a top layer;

forming a first mask layer over the covering layer;

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and first mask layer;

removing etch residue from the second mask layer and first mask layer; and

selectively wet removing the first mask layer by a process different than the same etching process, wherein the second mask layer remains.

36. (Original) The method of claim 35, wherein forming a first mask layer includes forming a first mask layer including titanium nitride.

37. (Original) The method of claim 36, wherein selectively wet removing the first mask layer includes selectively wet removing the first mask layer including an ammonium peroxide mixture wet removal.

38. (Original) The method of claim 37, wherein selectively wet removing the first mask layer further includes removing footings disposed adjacently to the first mask layer and second mask layer.

39. (Original) The method of claim 35, wherein selectively removing the first mask layer includes a process including plasma removal or ion milling.

40. (Currently Amended) The method of claim 35, wherein etching the second mask layer and first mask layer includes etching the second mask layer and partially etching the first mask layer, wherein the covering layer is not incorporated in an etch residue.

41. (Currently Amended) The method of claim 35, wherein forming a second mask layer includes forming a second mask layer including dielectric anti-reflective coating or ~~siline~~ silicon oxides.

42. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having a top layer;

forming a first mask layer over the covering layer;

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and first mask layer;

removing etch residue from the second mask layer and first mask layer; and

selectively wet removing the first mask layer by a process different than the same etching process, including removing footings disposed adjacently to the first mask layer and second mask layer, wherein the second mask layer remains.

43. (Original) The method of claim 42, wherein forming a first mask layer includes forming a first mask layer including titanium nitride.

44. (Original) The method of claim 42, wherein selectively wet removing the first mask layer includes selectively wet removing the first mask layer including an ammonium peroxide mixture wet removal.

45. (Currently Amended) The method of claim 42, wherein etching the second mask layer and first mask layer includes etching the second mask layer and partially etching the first mask layer, wherein the covering layer is not incorporated in an etch residue.

46. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having a top layer;

forming a first mask layer over the covering layer, wherein the first mask layer includes titanium nitride;

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and partially etching through the first mask layer, wherein the first mask layer separates the covering layer from etching;

removing etch residue from the second mask layer and first mask layer; and

selectively wet removing the first mask layer by a process different than the same etching process, including removing footings disposed adjacently to the first mask layer and second mask layer, wherein the second mask layer remains.

47. (Original) The method of claim 46, wherein etching the second mask layer and partially etching through the first mask layer includes preventing incorporation of the covering layer in an etch residue.

48. (Original) The method of claim 46, wherein selectively wet removing the first mask layer includes selectively wet removing the first mask layer including an ammonium peroxide mixture wet removal.

49. (Currently Amended) A method, comprising:

forming a substrate channel through a substrate;

providing a barrier over the substrate channel;

forming a conductor line over the barrier;

forming a first magnetic layer over the conductor line, barrier, and substrate;

forming a first interposing layer between the conductor line, barrier, and substrate and the first magnetic layer;

forming a second magnetic layer over the first magnetic layer;

forming a second interposing layer between the first magnetic layer and the second magnetic layer;

providing a covering layer over the magnetic layers;

forming a first mask layer over the covering layer;

forming a second mask layer over the first mask layer, wherein the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and partially etching the first mask layer, wherein the covering layer is not incorporated in an etch residue; and

selectively wet removing the first mask layer by a process different than the same etching process, including removing footings disposed adjacently to the first mask layer and second mask layer, wherein the second mask layer remains.

50. (Original) The method of claim 49, wherein providing a covering layer includes providing a covering layer including tantalum, and providing a first interposing layer includes providing a first interposing layer including tantalum.

51. (Original) The method of claim 49, wherein forming a first mask layer includes forming a first mask layer including titanium nitride.

52. (Original) The method of claim 51, wherein selectively removing the first mask layer includes selectively wet removing the first mask layer includes ammonium peroxide mixture wet removal.

53. (Currently Amended) The method of claim 49, wherein forming a second mask layer includes forming a second mask layer including dielectric anti-reflective coating or ~~siline~~ silicon oxides.

54. (Original) The method of claim 49, wherein providing a barrier over the substrate channel includes providing a barrier including tantalum, and forming a conductor line over the barrier includes forming a conductor line including copper.

55. (Original) The method of claim 49, wherein forming a second interposing layer between the first magnetic layer and the second magnetic layer includes forming a second interposing layer including a dielectric oxide layer.

56. (Currently Amended) A method, comprising:

providing a covering layer over an integrated circuit structure having magnetic layers;

forming a first mask layer over the covering layer, wherein the first mask layer includes titanium nitride;

forming a second mask layer over the first mask layer, wherein the second mask layer includes dielectric anti-reflective coating and the first mask layer and second mask layer are etchable by a same etching process;

etching the second mask layer and partially etching through a first mask layer, wherein the first mask layer separates the covering layer from etching, and the covering layer is not incorporated in an etch residue;

removing etch residue from the second mask layer and first mask layer; and

selectively wet removing the first mask layer using a process different than the same etching process, and the process includes an ammonium peroxide mixture, wherein the second mask layer remains.